UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,751	12/04/2003	Anthony R. Bonaccio	BUR9-2003-0099	3178

30449 7590 03/07/2007

SCHMEISER, OLSEN & WATTS
22 CENTURY HILL DRIVE
SUITE 302
LATHAM, NY 12110

EXAMINER	
BAE, JI H	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/729,751	BONACCIO ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-3,5-10,12-14 and 16-21* is/are rejected.

7)☒ Claim(s) *4,11,15,22,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

In response to applicant's arguments, new grounds of rejection are presented. Responses to applicant's specific arguments are embedded in rejections below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 9 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 9 recites that the fuse bank is coupled to the repair processor and is used to store information useable by said repair processor to implement a repair of said repairable circuit element. Applicant's specification teaches away from this usage [pp. 8, lines 11-16]. More specifically, applicant's specification teaches that the fuses determine connectivity between the replaced circuit and replacement circuit, and does not teach that fuse bank stores information used to repair the circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-7, 9, 10, 12-14, 16-18, 20, and 21. are rejected under 35 U.S.C. 103(a) as being unpatentable over Flower, U.S. Patent No. 5,688,232, in view of Daghighian, European Patent Application Publication No. 0204588 A2, in view of Carlson, U.S. Patent No. 6,861,865 B1.

Regarding claim 1, Flower teaches an integrated circuit comprised of a life cycle timer coupled to a controller [Fig. 2, controller ASIC 20, col. 4, lines 24-29], wherein the life cycle timer is used to determine that the controller has exceeded its useful life after a predetermine time [col. 3, lines 32-44]. Flower teaches that the life cycle timer is comprised of a clock [col. 3, line 33] which is started at the date of manufacture [line 34], stores a predetermined useful life time [col. 10, lines 18-20], determines when the continuous time from manufacture has exceeded the predetermined useful life time , and disables the controller [col. 10, lines 27-32].

Applicant has argued that Flower teaches neither a pulse generator nor a cycle counter [applicant's remarks, pp. 11]. As the examiner has shown, the life cycle timer of Flower clearly teaches a clock. The examiner concedes that what the "clock" of Flower comprises is not clear. However, the examiner submits that the following may be clearly discerned from Flower's teachings:

1. The clock/life cycle timer must be able to be activated at some point in time.
2. The clock/life cycle timer must be able to keep track of the cumulative time that has passed since activation.
3. The clock/life cycle timer must be able to discern when the cumulative time has reached a predetermined time, and disable the controller when the predetermined time limit has been reached.

The examiner submits that, based on the disclosed functionality, it would have been obvious to one of ordinary skill in the art that the life cycle timer would have been comprised of a clock [e.g. a standard oscillator] coupled a digital counter. Such a configuration is well-known in the art to accomplish the disclosed functions. Applicant's arguments that counting of radioactive decay emissions or measuring charge on a capacitor could have been used in the timer of Flower are not convincing given the context of Flower's disclosure – namely, a microprocessor-based ASIC with useful life times on the order of five years [col. 10, line 29]. Although the examiner submits that the configuration of a clock coupled to a counter is obvious to one of ordinary skill in the art, nevertheless the examiner concedes that a clock coupled to a counter is not explicitly taught in the reference.

Daghighian teaches a digital timer for use in a microprocessor that is clocked at a predetermined rate and is comprised of a counter. The counter counts until a predetermined time is reached, at which point an overflow signal is asserted. Daghighian teaches that the number of bits required for such a counter may vary depending on the counting range required [pp. 1, lines 12-21].

It would have been obvious to one ordinary skill in the art to combine Flower with Daghighian by implementing the life cycle timer of Flower as a counter clocked at a predetermined rate, as taught by Daghighian. Daghighian describes a set of operating parameters very similar to that of Flower – a timer used to determine when a predetermined time limit has been reached, asserting a signal when the limit has been reached. Moreover, Daghighian teaches that the configuration of a clock coupled to a counter is conventionally used in microprocessors and other similar devices. Since neither Flower nor Daghighian teaches away from the usage of a clock coupled to a counter (e.g. using a clocked counter would not be desirable for reasons X, Y, or Z), it would have been obvious to one of ordinary skill in the art to

use what is readily known. The examiner further notes that the improvements on the counter design taught by Daghighian do not teach away from the basic configuration of a counter coupled to a clock.

Thus, the combination of Flower and Daghighian teaches a pulse generator coupled to a cycle counter, and a circuit element that is disabled when a predetermined time limit has been reached, wherein the condition on the time limit being reached is determined by the life cycle timer comprised of a pulse generator and cycle counter. The examiner concedes that the combination of Flower/Daghighian does not expressly teach that the circuit element is repairable, and that repair is carried out when the time limit has been reached and before the circuit element fails.

Carlson teaches an integrated circuit comprising [Fig. 2a]:

one or more repairable circuit elements [logic blocks 200-203, 250]; and

a repair processor for repairing a repairable circuit element of said one or more circuit elements [col. 2, lines 1-6].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Carlson and Flower/Daghighian by implementing redundant circuit blocks, along with the means to repair them, in the system of Flower/Daghighian. Both Flower/Daghighian and Carlson are directed towards integrated circuits, and more specifically insuring failure-free operation. Flower teaches that integrated circuits have limited lifetimes, after which they must be discarded **or returned to the manufacturer for refurbishment** [col. 10, line32-34]. Clearly, Flower teaches that once the useful life time of the circuit has been reached, the circuit may continue to be used once it has been repaired. Since Carlson teaches a system for repairing an integrated circuit, the teachings of Carlson would improve the system of Flower by providing the repairing step that is required by the system of Flower [e.g. without having to return to the manufacturer for

refurbishment and without having to discard the system]. Additionally, the examiner points out that the useful life time limit of Flower implies that the time limit must be reached before product failure, since safety and product liability concerns necessitate the prevention of using a faulty device [col. 10, lines 38-41].

Regarding claim 2, Carlson teaches permanently disabling said repairable element and replacing it with a redundant circuit element [col. 3, line 62 to col. 4, line 10].

Regarding claim 3, Daghighian teaches that the pulsed signal is a clock signal.

Regarding claim 5, Flower teaches a trigger signal when said predetermined cycle count is reached [control signal, col. 3, line 43]. In the combination of Flower with Carlson, this control signal would indicate the expiration of the controller's lifetime, and thus trigger its replacement. Additionally, Daghighian teaches assertion of an overflow signal once a counter has counted to its predetermined value.

Regarding claim 6, Daghighian teaches an overflow signal once a counter has counted to its predetermined value. More specifically, an overflow signal for an N-bit counter is conventionally realized as the carry bit (or the N+1th bit) of the count value.

Regarding claim 7, the limitations recited are obvious in view of design choice. The inventive teachings could have been applied to any kind of circuit element.

Regarding claim 9, Carlson teaches a fuse bank [col. 3, line 3].

Regarding claim 10, Carlson teaches performing multiple repairs by repairing previously repaired circuit elements.

Regarding claims 12-14, 16-18, 20, and 21, Flower/ Daghighian/Carlson teach the integrated circuit of claims 1-3, 5-7, 9. and 10. Carlson and Flower also teaches the method implemented by the claimed circuit.

Claim 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flower/ Daghighian/Carlson as applied to claims 1 and 12 above, and further in view of Nogami et al, U.S. Patent No. 5,459,342.

Regarding claims 8 and 19, Flower/ Daghighian/Carlson teaches the circuit and method of claims 1 and 12, but does not teach that the circuit is implemented as an FGPA.

Nogami teaches an FPGA with spare circuit blocks that can be used to replace defective circuit blocks [abstract].

It would have been obvious to one of ordinary skill in the art to further modify Flower/ Daghighian/Carlson by implementing the system in an FGPA as taught by Nogami. Carlson teaches a series of replaceable logic blocks that can be selected by a bank of fuses, analogous to the FGPA taught by Nogami [col. 3 ,lines 7-20]. Thus Carlson suggests that the integrated circuit may be implemented as an FPGA. Additionally, FPGAs are well-known in the art for providing greater flexibility over hard-wired circuits, owing to their programmability.

Allowable Subject Matter

Claim 4, 11, 15, 22, 31, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
Art Unit 2115
ji.bae@uspto.gov
571-272-7181

CHUN CAO
PRIMARY EXAMINER